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Controlling Of Grid Interfacing Inverter Using ZVS Topology

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ABSTRACT
In a high-power grid-connected inverter application, the six-switch three-phase inverter is a preferred topology with several advantages such as lower current stress and higher efficiency. To improve the line current quality, the switching frequency of the grid-connected inverter is expected to increase. Higher switching frequency is also helpful for decreasing the size and the cost of the filter. However, higher switching frequency leads to higher switching loss. The soft-switching technique is a choice for a high-power converter to work under higher switching frequency with lower switching loss and lower EMI noise. The inverter can realize zero-voltage switching (ZVS) operation in all switching devices and suppress the reverse recovery current in all anti parallel diodes very well. And all the switches can operate at a fixed frequency with the new SVM scheme and have the same voltage stress as the dc-link voltage. In grid-connected application, the inverter can achieve ZVS in all the switches under the load with unity power factor or less. The aforementioned theory is verified in a 30-kW inverter. The reduced switching loss increases its efficiency and makes it suitable for practical applications.

Index Terms—Grid connected soft switching, space vector modulation (SVM), three-phase inverter, zero-voltage switching (ZVS).

I. INTRODUCTION

Several problems associated with hard switching are reported in the literature. The main problems are the semiconductor losses due to the finite duration of the switching transients and the electromagnetic compatibility (EMC) problems associated with the high voltage derivative with respect to time, occurring especially at the turn-off transient. Power electronic converter manufacturers strive towards increased switching frequencies in order to omit the audible noise and reduce the output current harmonic content. For such high switching frequencies, the switching losses dominate, at least if insulated gate bipolar transistor (IGBT) technology is employed. IGBT technology is the most common choice for mid-power converters due to its ease of drive, high ruggedness and favourable combination of moderate conduction and switching losses. In this paper, different means to achieve zero voltage switching (ZVS) are discussed. The aim is to perform the switching transients at, or close to, zero voltage across the semiconductor devices. At a first glance, this would give zero, or low, switching losses. However, this is not entirely true in the case of IGBTs and this is also discussed. The discussion treats the IGBT switching behaviour at hard-switched conditions, and with RCD charge-discharge snubbers, intended to provide zero voltage transistor turn-off. The resonant DC link (RDCL) converter investigated suffers from two severe drawbacks, both of which are highlighted. These drawbacks also put focus on quasi-resonant DC link (QRDCL) converters. An QRDCL converter is implemented and waveform and loss measurements are presented. Both RDCL and ACRDCL converters have to use discrete pulse modulation (DPM). DPM requires the dc-link resonating frequency to be several times higher than the switching frequency of the pulse width modulation (PWM) converter for similar current spectral performance [6], which normally causes undesirable sub harmonics. In [7], the PWM scheme is used to control the RDCL inverters, but the switching loss is increased, and the PWM range is also limited. The maximum voltage stress of the quasi-resonant dc-link PWM inverter (QRDCL) is only 1.01–1.1 times as high as the dc-bus voltage [8], [9]; however, the auxiliary device of QRDCL is normally in series with the dc bus causing higher conduction loss and switching loss, especially in high-power application. The PWM scheme can be used to control the QRDCL inverters, while normal PWM schemes still need to be modified in order to synchronize the turn-on events of main switches, which can increase the current ripple. The active-clamping ZVS-PWM half-bridge inverter. In an effort to improve the ZVS full-bridge PWM converter, a number of zero-voltage and zero-current switching (ZVZCS) full-bridge PWM converters have been proposed for the last several years [1-5]. The ZVS of the leading-leg switches is achieved by a similar manner as that of the conventional phase shifted ZVS full-bridge PWM converters, while the zero-current switching (ZCS) of the lagging-leg switches is achieved by resetting the primary current during the freewheeling period. In the previous works,

the ZVS operation of the ZVZCS full-bridge PWM converter has been known to be same with that of the ZVS full-bridge PWM converter, and only a few studies on the detailed analysis of the soft switching mechanism are found in the literatures. Since the ZVS mechanism of the ZVZCS full-bridge PWM converters is different from that of the conventional ZVS full-bridge PWM converter, different design considerations are required. The zero-current transition (ZCT) inverter [20]–[22] achieves ZCS in all of the main and auxiliary switches and their anti parallel diodes. This topology needs six auxiliary switches and three LC resonant tanks. The simplified three-switch ZCT inverter [23] needs only three auxiliary switches to achieve zero-current turn-off in all of the main switches and auxiliary switches. Compared with the six-switch ZCT inverter, the resonant tank current stress of the three-switch ZCT inverter is higher. The structure of the ZVS-SVM controlled three-phase PWM rectifier [24] is similar to the ACRDCL converter. With the special SVM scheme proposed by the authors, both the main switches and the auxiliary switch have the same and fixed switching frequency. The reverse recovery current of the switch antiparallel diodes is suppressed well and all the switches can be turned ON under the zero-voltage condition. Moreover, the voltage stress in both main switches and the auxiliary switch is only 1.01–1.1 times of the dc-bus voltage. In this paper, a ZVS three-phase grid-connected inverter is proposed. The topology of the inverter is shown in Fig. 2, which is similar to the rectifier topology proposed in [24]. All the soft-switching advantages under the rectifier condition can be achieved in a grid-connected inverter application, and the voltage stress in both main switches and the auxiliary switch is the same as the dc-bus voltage. The operation principle of this SVM scheme is described in detail.

II. INVERTER TOPOLOGY AND MODULATION SCHEME

In fig 2 it is shown the basic PWM inverter circuit and the clamped circuit. The clamping circuit consists of active switch S7, resonant inductor Lr , and clamping capacitor Cc . During most time of operation, the active switch S7 is in conduction mode, and energy circulates in the clamping branch. When the auxiliary switch S7 is turned OFF, the current in the resonant inductor iLr will flow through the parallel capacitors of the main switch and then the main switch can be turned ON under the zero-voltage switching condition. When the main switch is turned ON, Lr eliminates the reverse recovery current of an anti parallel diode of the other main switch on the same bridge. Since it is a two level inverter, normally the auxiliary switch must be activated three times per PWM cycle if the switch in the three legs is modulated asynchronously. To make the auxiliary switch having the same switching frequency as the main switch, a new type of Space vector modulation scheme is proposed to control the inverter. Suppose that the grid-connected inverter works with unity power factor; the grid line voltage and the inverter output current waveform are shown in Fig. 3; the corresponding voltage sector definition is shown in Fig. 4.

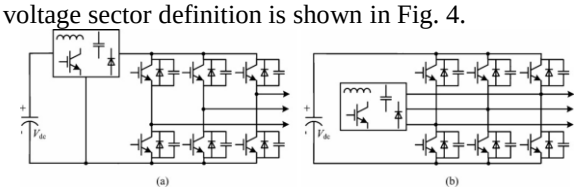


Fig. 1. Soft-switching three-phase inverter topology: (a) dc-side topology and (b) ac-side topology

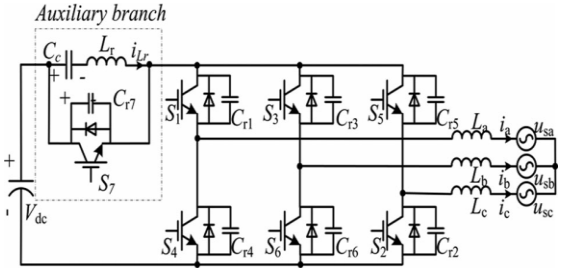


Fig. 2. ZVS three-phase inverter

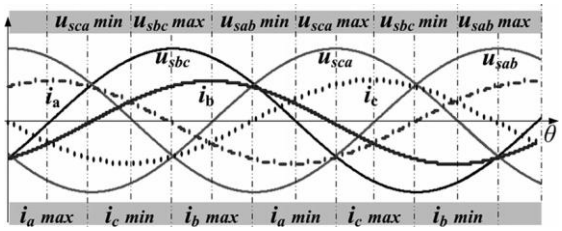


Fig. 3. Grid line voltage and inverter output current waveform.

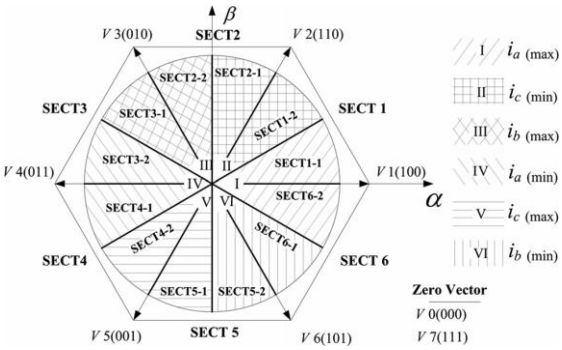


Fig. 4. Grid voltage and inverter current space vector diagram

In voltage SVM, the whole utility cycle can be divided into six voltage sectors, and every grid voltage sector can still be divided into two different smaller sectors according to the maximum value of the phase current in the inverter. For example, the grid voltage sector SECT1 can be divided into SECT1-1

and SECT1-2. In SECT1-1, the absolute value of the phase-A current obtains the maximum value, and in SECT1-2, the absolute value of the phase-C current does the same. Since the operation of the converter is symmetrical in every 30◦, assume that the inverter is operating in SECT1-1. If the grid-connected inverter works with unity power factor, ia > 0 and ic < ib < 0 in SECT1-1. The phase voltage and phase current in phase A obtains the maximum value; there exist four switching states as shown in Fig. 4: 111, 100, 110, and 000. The equivalent circuits of these four switching states are shown in Fig. 5. If the switching sequence in SECT1-1 is 111-100-110-111, as shown in Fig. 6, then the zero vector will always be 111 and switch S1 will always be in conduction. When the switching state changes from 111 to 100, switches S6 and S2 will be turned ON simultaneously. The auxiliary branch needs to act in this transition process to suppress the reverse recovery currents of antiparallel diodes of S3 and S5 and create the ZVS condition for S6 and S2 . During the state from 100 to 110, the current in S6 at first will flow into the anti parallel diode of S3. During the state from 110 to 111, the current in S2 will flow into the anti parallel diode of S5 . These two transitions are normal soft switching. Thus, the auxiliary branch only needs to act once in one switching cycle to resonant the dc bus to zero, creating the ZVS condition for the switches and suppressing the diode recoveries in two phases. The auxiliary switch can work at the same frequency as the main switch. And the main switch can be turned ON or OFF at the exact time decided by the SVM control. The resonant process equivalent circuits in the state change from 111 to 100 as shown in Fig. 5. The key waveform of the inverter equivalent circuit in SECT1-1 is shown in Fig. 6. Take SECT1-1 as an example for analysis, the steady-stage circuit and key waveforms of the inverter are shown in Figs. 6, respectively. During circuit topological changes, the complete circuit operation in SECT1-1 can be divided into nine stages.

The following assumptions are made to simplify the analysis of the ZVS inverter:

1) Switches S1–S7 are considered as an ideal switch with its anti parallel diode;

2) Capacitances Cr 1–Cr 7 paralleled with switches S1–S7, respectively, include parasitic capacitance and external capacitance;

3) In one switching cycle, the inductor current ripple is small and can be considered as a constant current source;

4) The capacitance of the clamping capacitor Cc is large enough, so the voltage ripple across it is small, and thus can be regarded as a voltage source;

5) The resonant frequency of Cc and Lr is much lower than the operation frequency of the converter.

Stage 1 (t0 –t1): Main switches S1, S3 , and S5 and auxiliary switch S7 are ON. The circuit is in the state 111. In the auxiliary resonant cell, the voltage of Lr is clamped by clamping capacitor Cc , and its current iLr increases at the rate of

$$\frac{dirl}{dt} = -\frac{Vce}{Lr} \quad (1)$$

Stage 2 (t1 –t2): In t1, S7 is turned OFF; the resonant inductor Lr discharges the parallel capacitors Cr 4 , Cr 6 , and Cr 2 and charges parallel capacitor Cr 7 of the auxiliary switch S7. S7 is turned OFF under the ZVS condition because of the snubber capacitor Cr 7 .

Stage 3 (t2 –t3): In t2 , the voltage across S7 reaches Vdc, S7 is OFF, the voltages across Cr 4 , Cr 6 , and Cr 2 drop to zero, and the antiparallel diodes of these main switches start to conduct. The resonant between Lr and these paralleled capacitors stops. S2 and S6 can be turned ON under the ZVS condition.

Stage 4 (t3 –t4): In t3, S2 and S6 are turned ON under the ZVS condition. In this stage, the currents in phase B and phase C convert from the antiparallel diodes of S3 and S5 to S2 and S6 , respectively. When the main switch transition process completes, the antiparallel diodes of S3 and S5 experience diode reverse recovery. Due to the existence of the resonant inductor Lr , the diode reverse recovery is suppressed and the current in Lr iLr changes at the rate of

$$\frac{dlr}{dt} = \frac{Vde - Vce}{Vr} \quad (2)$$

Stage 5 (t4 –t5): Main switches S3, S4 , and S5 are OFF at t4 ; the circuit reaches the state 100. Lr , Cr 3 , Cr 4 , Cr 5 , and Cr 7 start to be in resonance. The voltages across S3, S4 , and S5 start to increase and the voltage across S7 starts to decrease. At t5, the voltages across S2, S4 , and S6 reach to Vdc, the voltage across S7 decreases to zero, and the antiparallel diode of S7 starts to conduct. S7 can be turned ON under the ZVS condition. Lr , Cr 3 , Cr 4 , Cr 5 , and Cr 7 stop to be in resonance. The time between t2 and t5 is the duty cycle loss of S2 and S6 . As stages 3–5 are very short compared with the whole switching cycle, the impact of this duty cycle loss on the circuit operation during the whole switching cycle can be ignored.

Stage 6 (t5 –t6): At t5 , the circuit reaches the state 100. The main switches S1, S2 , and S6 and the auxiliary switch S7 areON. The resonant inductor is charging the clamping capacitor Cc .

Stage 7 (t6 –t7): At t6, S6 is turned OFF. The inductor Lb will charge C6 and discharge C3 . Due to the existence of C3 and C6 , S6 is turned OFF under the ZVS condition. Stage 8 (t7 –t8): The circuit reaches the state 110. The main switch S1, S3 , and S2 and the auxiliary switch S7 are ON. The resonant inductor is charging the clamping capacitor Cc

Stage 9 (t8 –t9): At t7, S2 is turned OFF. The inductor Lc will charge C2 and discharge C5 . Due to the existence of C5 and C2 , S2 is turned OFF under the ZVS condition. At t9 , the voltage on S5 decreases to zero, and the antiparallel diode of S5 starts to

conduct. S6 can be turned ON under the ZVS condition. The circuit reaches the state 100. After t 9 , a new switching cycle starts again.

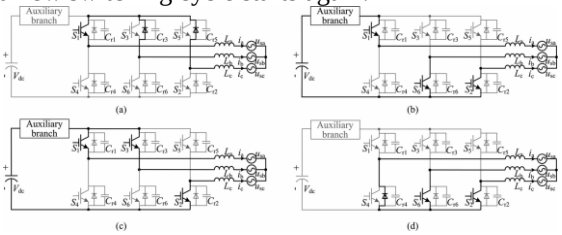


Fig. 5. Four switching states in the SECT1-1: (a) state 111, (b) state 100, (c) state 110, and (d) state 000.

III. MODULATION SCHEME UNDER DIFFERENT CURRENT POWER FACTORS

The aforementioned analysis is based on the assumption that the grid-connected inverter works with unity power factor. Actually, the ZVS inverter can still work when □u ≠ □i ; the corresponding voltage sector definition is shown in Fig. 4. The grid

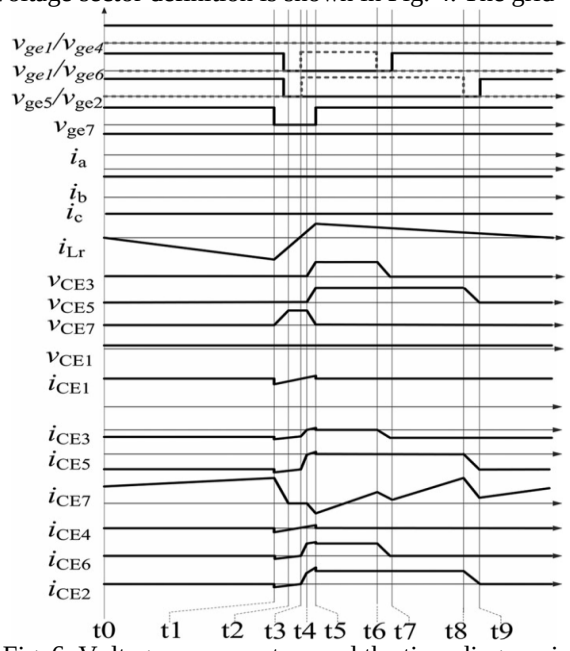


Fig. 6. Voltage space vectors and the time diagram in SECT1-1.

Voltage and inverter current are expressed, respectively, as

$$Usa = Uscos(wt + \Psi u) \quad (3)$$

$$Usb = Uscos\left(wt - \frac{2pi}{3} + \Psi u\right) \quad (4)$$

$$Usc = Uscos\left(wt + \frac{2pi}{3} + \Psi u\right) \quad (5)$$

$$Isa = Iscos(wt + \Psi u) \quad (3)$$

$$Isb = Iscos\left(wt - \frac{2pi}{3} + \Psi u\right) \quad (4)$$

$$Isc = Iscos\left(wt + \frac{2pi}{3} + \Psi u\right) \quad (5)$$

Take |Wu− W i| ≤ π/6 for example; the auxiliary switch S7 only needs to act once in one switching cycle to resonant the dc bus to zero, creating the ZVS condition for switches and suppressing the diode recoveries in two phases. The auxiliary switch can work at the same frequency as the main switch. And the main switch can be turned ON or OFF at the exact time decided by the SVM control. The modulation scheme of the main switch with |□u − □i| ≤ π/6 is shown in Table I.

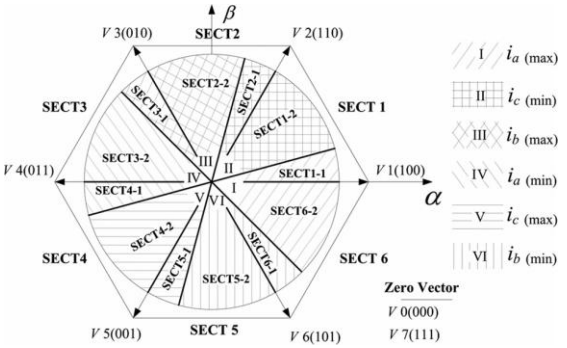


Fig. 7. Grid voltage and inverter current space vector diagram (PF ≠ 1).

IV. SIMULATION AND MATLAB IMPLEMENTATION

A 30-kVAv three-phase two level soft-switching grid connected inverter and control structure is implemented using Matlab/ simulation software and is tested in different power factors as shown in Fig. 1, The parameters considered for the circuit are of the circuit are Vdc = 680V, grid phase voltage 220Vrms, the output filter inductor L=0.3 mH, the resonant capacitance Cr = 3.3 nF, the resonant inductance Lr 30 μH, and the operation frequency f = 16 kHz.

TABLE I
SWITCHING SEQUENCE OF THE ZVS INVERTER

sector	Voltage vector angle	Zero vector	First vector	Second vector	Zero vector
SECT6-2	$11\pi/6+\varphi_i-\varphi_u$~$2\pi$	1 1 1	1 0 0	1 0 1	1 1 1
SECT1-1	0~$\pi/6+\varphi_i-\varphi_u$	1 1 1	1 0 0	1 1 0	1 1 1
SECT1-2	$\pi/6+\varphi_i-\varphi_u$~$\pi/3$	0 0 0	1 1 0	1 0 0	0 0 0
SECT2-1	$\pi/3$~$\pi/2+\varphi_i-\varphi_u$	0 0 0	1 1 0	0 1 0	0 0 0
SECT2-2	$\pi/2+\varphi_i-\varphi_u$ ~$2\pi/3$	1 1 1	0 1 0	1 1 0	1 1 1
SECT3-1	$2\pi/3$~$5\pi/6+\varphi_i-\varphi_u$	1 1 1	0 1 0	0 1 1	1 1 1
SECT3-2	$5\pi/6+\varphi_i-\varphi_u$ ~π	0 0 0	0 1 1	0 1 0	0 0 0
SECT4-1	π~$7\pi/6+\varphi_i-\varphi_u$	0 0 0	0 1 1	0 0 1	0 0 0
SECT4-2	$7\pi/6+\varphi_i-\varphi_u$ ~$4\pi/3$	1 1 1	0 0 1	0 1 1	1 1 1
SECT5-1	$4\pi/3$~$3\pi/2+\varphi_i-\varphi_u$	1 1 1	0 0 1	1 0 1	1 1 1
SECT5-2	$3\pi/2+\varphi_i-\varphi_u$ ~$5\pi/3$	0 0 0	1 0 1	0 0 1	0 0 0
SECT6-1	$5\pi/3$~$11\pi/6+\varphi_i-\varphi_u$	0 0 0	1 0 1	1 0 0	0 0 0

Fig. 8 shows the grid voltage and the phase current of the ZVS grid-connected inverter under different power factors. The phase THDi of the ZVS grid-connected inverter under 30-kW output power is 3.3%, which is similar to that of the hard switching inverter. It means that there is a slight influence of the auxiliary resonance branch to the inverter output voltage and current quality.

The waveforms of the collector–emitter (CE) voltage and the conduction current of the main switch S6 in SECT1-1 are shown in Fig. 9. The positive reference direction of the insulated gate bipolar transistor (IGBT) conduction current is from the collector to the emitter. It can be seen from Fig. 9 that the CE voltage of the main switch is clamped to zero before the main switch is turned ON, and then the ZVS turn-on of the main switch is realized.

The waveforms of the CE voltage and the conduction current of the antiparallel diode of the main switch S6 in SECT1-1 are shown in Fig. 10. It can be seen from Fig. 16 that the reverse recovery current of the antiparallel diode has been suppressed well.

The waveforms of the auxiliary switch current and voltage are shown in Fig. 11. It can be seen from Fig. 11 that in most time of a switching cycle, the auxiliary switch S7 is ON; then the duty cycle loss of main switches is small compared with the whole switching cycle. The resonant branch current and auxiliary switch voltage are shown in Fig. 12. It can be seen from Fig. 13 that the current of the resonant inductor is symmetrical high-frequency current. The mean value of the current in S7 is equal to the mean value of ibus. It means that the larger the inverter's output power, the more the conduction losses of auxiliary switch S7.

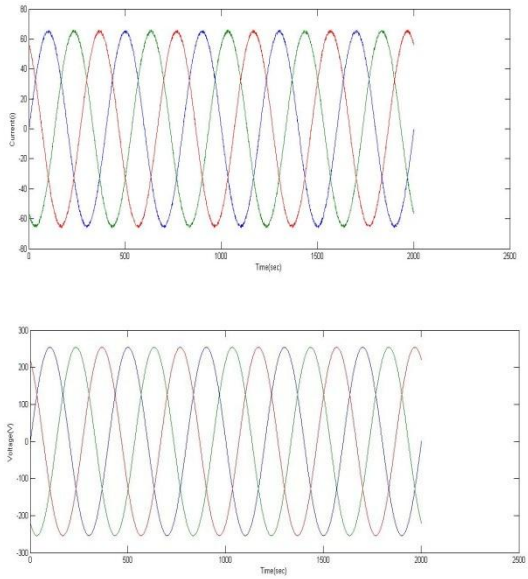
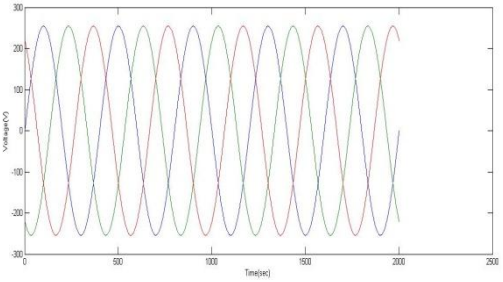


Fig 8(a) $\varphi u = \varphi i$,



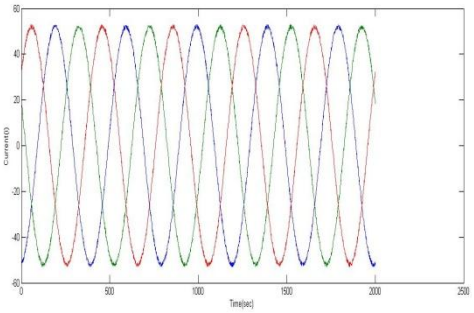
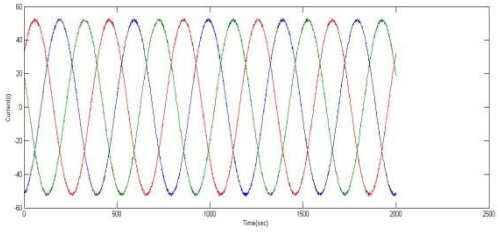


Fig 8(b), $\varphi u - \varphi i = -\pi/6$,



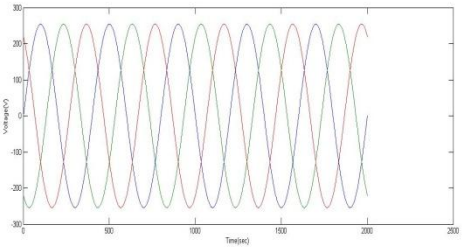


Fig 8(c) $\varphi u - \varphi i = \pi/6$.

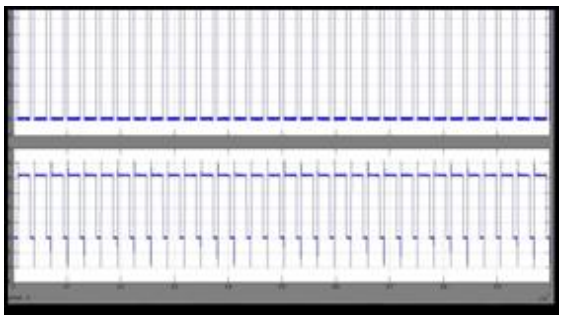


Fig 9 CE voltage and current of S6 (IGBT on)

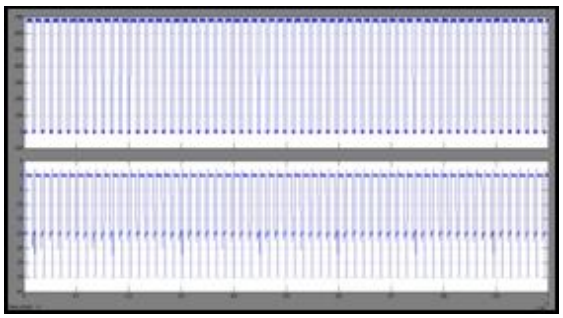


Fig 10CE voltage and current of S6 (diode on)

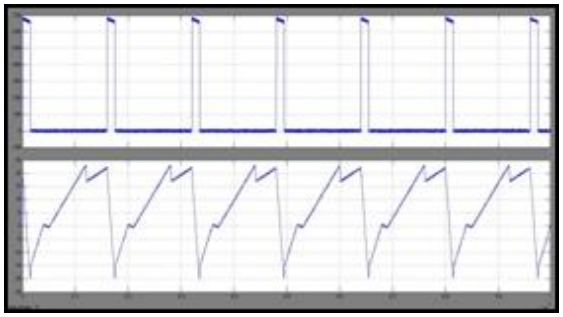


fig 11 CE voltage and current of S7

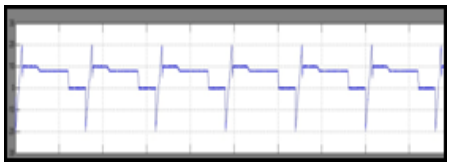
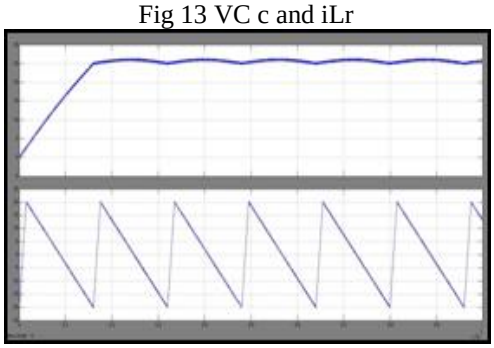


Fig 12 Ibus

Fig 13 VC c and iLr



V. CONCLUSION

The simulation analysis verified using different power factors with the SVM-controlled three-phase soft-switching grid-connected inverter. it is observed that the ZVS operation for all switching devices, and the reverse recovery current in the anti parallel diodes of all switching devices is suppressed well. SVM can be realized at the fixed switching frequency. And the switching voltage stress across all the power switch devices is the same as the dc-link voltage. The ZVS can be achieved in the grid-connected ZVS inverters under the load with unity power factor or less. The reduced switching loss increases its efficiency and makes it suitable for practical applications. and further paper can be extended using multi level inverter.

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